REPLACEMENT CLAIMS

19. (amended) A dual damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

a second insulating layer provided over said metal layer;

a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with a titanium-silicon-nitride layer and filled with a copper material;

a third insulating layer located over said second insulating layer;

a trench situated within said third insulating layer and extending to said via, said trench being lined with said titanium-silicon-nitride layer and filled with said copper material.

20. (amended) The dual damascene structure of claim 19, wherein said second insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

21. (amended) The dual damascene structure of claim 19, wherein said second insulating layer includes silicon dioxide.

22. (amended) The dual damascene structure of claim 19, wherein said second insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

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23. (amended) The dual damascene structure of claim 19, wherein said third insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

24. (amended) The dual damascene structure of claim 19, wherein said third insulating layer includes silicon dioxide.

25. (amended) The dual damascene structure of claim 19, wherein said third insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

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30. (amended) The dual damascene structure of claim 19, wherein said substrate is a silicon substrate.

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31. (amended) A damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

at least another insulating layer provided over said metal layer; and

at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material.

32. (amended) The damascene structure of claim 31, wherein said at least another insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

33. (amended) The damascene structure of claim 31, wherein said at least another insulating layer includes silicon dioxide.

34. (amended) The damascene structure of claim 31, wherein said at least another insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

39. (amended) The damascene structure of claim 31, wherein said substrate is a silicon substrate.

40. (amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure, said damascene structure comprising a metal layer provided within a first insulating layer formed over a substrate, at least another insulating layer provided over said metal layer, and at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with copper.